TECHNICAL DEEP-DIVE

Loss Analysis of the IBC DCX Transformer in the 800V HVDC → 48V → Core AI-Server Power Chain

Why magnetic loss — not copper loss — governs the 48V→12V intermediate-bus stage, and why classic Steinmetz gets it wrong.

Application: AI-server power (AIDC) · Intermediate Bus Converter (IBC) · 48V→12V DCX/LLC stage **Type:** Selection & design report

01 Key Takeaways

When 800V HVDC becomes the backbone of AI data-center power, many engineers assume the 48V stage will be marginalized. The opposite is true: 48V remains the fixed distribution rail for IT loads, and the Intermediate Bus Converter (IBC) that performs 800V/400V → 48V → 12V is the single stage where transformer loss concentrates — and where it is most often mis-estimated. This report focuses on the DCX (DC transformer, fixed-ratio open-loop / quasi-resonant stage) and presents three counter-intuitive conclusions that decide whether the thermal budget holds.

Three Counter-Intuitive Conclusions

- **#1:** DCX is magnetic-loss dominated, not copper-loss dominated. A fixed turns ratio plus near-square-wave excitation drives winding RMS current very low, shifting the loss center from I²R to the core's B-H hysteresis/eddy loss — the reverse of ordinary power-inductor intuition.
- **#2:** Classic sinusoidal Steinmetz can mis-estimate DCX core loss — but only in specific conditions. At exactly 50% duty (symmetric triangular flux) the two agree closely; the underestimate of 15%–40% appears when duty departs from 50% or when SiC/GaN fast edges concentrate the flux change into a narrow window, raising local dB/dt. iGSE (improved Generalized Steinmetz) is then required, or the temperature-rise budget is blown.
- **#3:** DCX runs at symmetric small flux swing with virtually no DC bias, so material selection is inverted: favor low-loss MnZn ferrite over high-Bs nanocrystalline/metal powder. Chasing high saturation flux density here is wasteful and runs hotter.

02 Power-Chain Context: 800V HVDC → 48V → Core

Before analyzing DCX loss, it must be placed back into the full chain. A typical AI-training rack is powered from an 800V HVDC bus and stepped down stage by stage to roughly 0.8V at the GPU core. The magnetic-loss mechanism at each stage is fundamentally different; conflating them is exactly why most loss analyses stay superficial.

Stage	Conversion	Key magnetic	Dominant loss mechanism (distinct)
①	800V HVDC → 48V	Isolated DC-DC / resonant inductor	HV isolation & insulation margin; mid-high-freq resonance
②	48V → 12V (IBC)	DCX / LLC transformer	Fixed ratio, near-square excitation → CORE loss dominated (this report)
③	12V → 0.8V (VRM)	Coupled inductor / TLVR	Large DC bias + high ripple → AC winding loss + DC-bias soft saturation
④	Transient / decoupling	Chip inductor, beads	High-freq loss, EMI suppression

Why the IBC stage gets harder, not easier, in the 800V era

A common misconception: since the upstream rose to 800V, the 48V segment should see lower stress. But rack compute density (already past 100kW per rack and trending toward 1MW) grows faster than the voltage step-up, so the total power carried by the 48V rail rises rather than falls. The IBC stage must therefore

perform 48V→12V conversion at higher power density in a tighter envelope — window area and cooling space shrink, core-loss density (mW/cm³) climbs, and temperature rise is amplified. In short, 800V HVDC does not make the IBC transformer easier; it pushes it toward a harsher loss-versus-thermal boundary. That is why the full chain is treated here only as context, with the engineering depth concentrated on stage ② — the DCX transformer, ProMagTech's most differentiated stage in AI-server magnetics.

03 DCX Operating Principle & Loss-Center Shift

A DCX (DC transformer) is an isolated converter operating at a fixed turns ratio and fixed (or near-fixed) duty, typically realized as an open-loop or fixed-frequency resonant LLC. Its goal is not regulation but to act as an efficient DC transformer — converting the 48V rail by ratio N:1 (commonly 4:1) to 12V, with voltage regulation handled upstream or downstream.

Why the loss center shifts from I²R to the core

- Fixed ratio + fixed duty means primary/secondary current waveforms approach an ideal square wave, with a low RMS factor; in a good design copper loss can be under 40% of the total.
- Square/trapezoidal voltage applied to the magnetizing inductance produces a triangular flux swing. The core completes one symmetric B-H loop per switching cycle, making hysteresis + eddy loss the dominant term.
- Consequently the DCX loss budget must be built around the core, not the windings — the exact opposite of ordinary DC power-inductor intuition, and the first mistake new engineers make.

Loss-Structure Contrast

- **Ordinary power inductor:** Large DC component + small ripple → winding I²R and DC-bias soft saturation dominate; core loss secondary. Material leans to high-Bs (FeSi / Sendust powder).
- **DCX transformer:** No DC bias + symmetric large swing + near-square → core hysteresis/eddy loss dominates; winding RMS low. Material leans to low-loss MnZn ferrite.

04 Core Insight: Steinmetz Fails Under Square-Wave Excitation

This is the technical heart of the report — and the engineering trap most generic loss analyses never touch. Core-loss estimation routinely uses the Steinmetz equation Pv = k·f^α·B^β, but its coefficients k, α, β are fitted under sinusoidal excitation. DCX magnetizing voltage is a square wave and the flux is triangular; dB/dt is piecewise-constant rather than smoothly sinusoidal — applying sinusoidal coefficients systematically understates core loss.

Physical root: loss is non-linearly sensitive to dB/dt

Eddy-current and part of the residual loss scale roughly with a power of dB/dt. One detail must be stated honestly: at exactly 50% duty with a symmetric triangular flux, the square-wave and sinusoidal equivalent losses are actually close (iGSE/sine ≈ 0.9–1.0) — there is no large underestimate. The real underestimate arises in two cases: (1) duty clearly departs from 50%, so volt-second balance makes the rising/falling flux segments asymmetric and the steep segment's dB/dt rises; and (2) SiC/GaN fast switching concentrates the flux change into a narrow edge window (trapezoidal / fast-edge), pushing local dB/dt far above the sinusoidal case. Only then does sinusoidal Steinmetz systematically understate, by up to 15%–40%. The root cause is not the "square-wave" label but the local steepness of dB/dt and the departure from 50% duty.

Engineering correction: iGSE (improved Generalized Steinmetz)

iGSE drops the sinusoidal assumption and integrates the actual dB/dt waveform piecewise, using a coefficient ki (analytically derived from k, α, β) to compute per-cycle loss. Its form integrates |dB/dt|^α · (ΔB)^(β−α) over one period. For the triangular flux of a DCX it expands analytically, giving a higher, measurement-consistent loss figure than sinusoidal Steinmetz.

Aspect	Classic Steinmetz (sine)	iGSE (actual waveform)
Excitation assumption	Sinusoidal V / flux	Arbitrary waveform, piecewise dB/dt
DCX applicability	Systematically underestimates	Tracks square-wave measurement
Typical deviation	Symmetric triangle ~±10%; off-duty/ fast-edge understates 15%–40%	Reference baseline
Engineering consequence	Thermal budget blown, overheating risk	Cooling margin trustworthy
Data needed	Vendor sinusoidal Pv curves	Same k/α/β converted to ki

Criterion Trap

- **Trap:** Multiplying the datasheet sinusoidal Pv@100kHz by volume and calling it DCX core loss — the number-one cause of runaway thermal budgets.
- **Correct approach:** Use iGSE: convert the same Steinmetz coefficients into ki and compute against the real duty and triangular flux waveform; evaluate the duty-far-from-50% case separately, since larger deviation raises the square-wave-equivalent loss.
- **Note:** Duty, dead-time and resonant operating point all reshape the flux waveform; evaluate at the true operating point, not the datasheet nominal. Figures are public engineering references, to be confirmed per project.

04+ Worked Example: A 48V→12V DCX Core-Loss Walkthrough

To ground the method in numbers, here is a self-consistent set of public reference conditions (not ProMagTech measured data). The goal is to show how the calculation is done, and when — and by how much — sinusoidal and iGSE results diverge. All values must be re-checked against the real project.

Step 1 — Define the example operating point

Parameter	Example value	Note
Input / output	48V → 12V	Turns ratio N = 4:1
Topology / excitation	Half-bridge DCX, primary ≈ 24V	Near-square voltage, triangular flux
Switching freq fsw	400 kHz	Mainstream for high-frequency AI-server IBC
Example power	~1 kW (per module)	For order-of-magnitude only
Core (example)	Planar MnZn (PC95 class)	Ae ≈ 120 mm², Ve ≈ 10 cm³
Primary turns Np	2 T	Example value

Step 2 — Solve for peak-to-peak flux ΔB

From volt-second balance ΔB = V·t /(Np·Ae). With half-period t = 1/(2·fsw) = 1.25 µs and primary voltage ≈ 24V, this gives ΔB ≈ 0.15 T (Bpk ≈ 0.075 T) — well within the low-loss high-frequency window of MnZn ferrite and far from saturation.

Step 3 — Compute loss with sinusoidal Steinmetz vs iGSE

Holding ΔB = 0.15 T fixed and varying only duty and edge steepness isolates the waveform effect. The table

states the honest result: at D = 0.5 (symmetric triangle) the two are nearly identical; the underestimate only becomes significant at off-duty or fast-edge conditions.

Condition (ΔB fixed at 0.15T)	iGSE / sine ratio	Sine underestimate
Duty D = 0.5 (symmetric triangle)	≈ 0.92×	None (slightly over-estimates)
Duty D = 0.3	≈ 0.98×	≈ 2%
Duty D = 0.2	≈ 1.07×	≈ 7%
Duty D = 0.15	≈ 1.16×	≈ 14%
Duty D = 0.10	≈ 1.32×	≈ 24%
Fast edge / trapezoidal (SiC/GaN, change in first 50% of window)	≈ 1.27×	≈ 21%
Steeper edge (first 30%)	≈ 1.60×	≈ 38%

Three Engineering Conclusions from the Example

- **#1:** At the nominal symmetric point (D=0.5), agonizing over sine vs iGSE adds little — they agree. This step actually validates that your datasheet core loss is trustworthy at that point.
- **#2:** The real risk is off-nominal: duty departing from 50%, or SiC/GaN fast switching steepening the flux edge, is where sinusoidal Steinmetz begins to systematically understate — up to ~38%.
- **#3:** Practice: estimate quickly from the datasheet at the nominal point, but re-check the worst-case (steepest edge / most off-duty) operating point with iGSE, and size the thermal budget to the worst case, not the nominal.

⚠ **Example disclaimer:** the Ae, Ve, turns and Steinmetz coefficients above are public order-of-magnitude references used to demonstrate the calculation method and the divergence trend — not ProMagTech measured data. The specific core grade, loss coefficients and operating point must be measured/verified per customer project.

05 Material Trade-off for the DCX Symmetric Small-Swing Regime

Because DCX is core-loss dominated, has almost no DC bias, and runs at a symmetric flux swing, its material logic differs sharply from a power inductor. The table contrasts three common core materials specifically for the DCX (48V→12V, ~100–500kHz) regime, rather than listing generic datasheet parameters.

Material	MnZn ferrite	Nanocrystalline (ribbon)	FeSi / Sendust powder
Saturation Bs (ref.)	~0.40–0.51 T	~1.2 T	~1.5–1.6 T
High-freq core loss	Low (optimized for HF)	Medium (needs thin ribbon, good insulation)	High (intrinsic powder loss)
DCX suitability	★★★★★ first choice	★★★ HF special case	★ not recommended
Why	No DC bias → high Bs useless; low loss is what matters	High Bs but loss & cost rise; only for extreme HF / miniaturization	Built to resist DC bias — irrelevant to DCX, yet carries high loss
Temp / Curie	Tc ~200–230°C	High Tc, good thermal stability	Grade-dependent, soft saturation

Key judgment: with no DC bias, the very advantage that justifies metal-powder cores — soft saturation and DC-bias tolerance — is useless in a DCX, while their higher intrinsic loss becomes a liability. This is a textbook case of higher-Bs-is-not-better: selection should return to loss density and temperature rise, not saturation flux density.

06 Planar vs Wire-Wound Transformer

In AI servers, a DCX often faces a choice between planar (PCB-embedded windings) and conventional wire-wound construction. Each carries trade-offs in loss, cooling and consistency — no absolute winner, only a match to the operating point.

Dimension	Planar transformer	Wire-wound transformer
AC winding loss	Layer stack controllable, proximity effect optimizable, but inter-layer design must be precise	Litz wire can suppress proximity effect, but termination & stacking depend on craft
Cooling	Flat, large area, easy to heat-sink, low thermal resistance	Concentrated volume, hot spots harder to extract
Consistency / batch	High PCB repeatability, suited to volume	Depends on winding craft and operator/ machine consistency
Turns / ratio flexibility	High turn count limited by PCB layers	Flexible turns, easy high ratios
LV high-current secondary	Excellent (copper foil / PCB planar conductor)	Needs multi-strand parallel, complex terminations
Recommendation	HF, low ratio, high current, volume (common first choice for 48V→12V DCX)	High ratio, custom, low volume or special structure

ProMagTech Engineering View

- **Selection logic:** 48V→12V DCX is a low-ratio, low-voltage high-current, high-frequency, volume scenario where planar excels at secondary current and cooling — but the planar option's inter-layer AC loss and proximity effect must be modeled during stack-up design, not patched afterward.
- **What we do:** Loss-thermal co-design for flat-wire / planar windings, with turns-ratio and window-utilization assessment per the customer's operating point. Exact parameters depend on the customer topology, frequency and duty.

07 Pitfalls, Failure Modes & Extended FAQ

Common pitfalls and failure modes

- Pitfall 1 — sinusoidal Pv for core loss: thermal budget blown, long-term overheating, loss worsens with temperature creating positive feedback (a thermal-runaway precursor).
- Pitfall 2 — duty far from 50% not separately checked: larger deviation, higher square-wave-equivalent loss; nominal looks fine while the real operating point overheats.
- Pitfall 3 — high-Bs powder cores chosen for margin: DCX has no DC bias, so this only adds loss and temperature rise — losing on both volume and cost.
- Failure mode — runaway inter-layer AC loss in planar: proximity effect amplified across stacked layers, local copper hot spots age the insulation.
- Failure mode — secondary high-current termination hot spots: at low voltage and high current, termination resistance and contact thermal resistance become hidden loss sources to address at layout/terminal stage.

Extended FAQ

Q: Are DCX and LLC transformers the same thing?
A: DCX is a usage/role — a fixed-ratio, non-regulating DC transformer; LLC is a topology/means. Open-loop or fixed-frequency LLC is often used to realize a DCX. The loss conclusions here apply generally to resonant-realized DCX.

Q: Why not use nanocrystalline to shrink the size?
A: Nanocrystalline's high Bs helps miniaturization, but in the DCX's no-bias, loss-dominated regime its higher HF loss and cost usually offset the volume gain. Worth weighing only at very high frequency or extreme miniaturization with adequate cooling.

Q: iGSE is complex — any engineering shortcut?
A: For standard square-wave excitation, iGSE expands analytically for triangular flux as a function of duty, collapsing to a correction factor. Build a one-time lookup/conversion and call it by operating point instead of numerically integrating each time.

Q: How high should the efficiency target be at this stage?
A: As a DC transformer in the main power path, DCX commonly targets 98%+ — 0.5% of loss on a 100kW rack is hundreds of watts of heat. Every loss term is worth chasing, and the core is the first.

Q: How does this relate to your LLC frequency-knee article?
A: That piece covers beyond-the-knee, volume benefit goes sub-linear while total loss rises; this report covers at-the-same-frequency, the wrong waveform assumption understates core loss. One is the frequency axis, the other the waveform axis — complementary.

Q: Can I copy these parameters into my design?
A: No. All values here are material-standard / public engineering references illustrating mechanism and order of magnitude. Actual ratio, frequency, duty and core grade must be confirmed against your topology and operating point — send us your conditions for evaluation.

08 Related Resources & Contact

This report complements the following articles in the ProMagTech technical library — cross-reading recommended:

- "The 400kHz Frequency Knee in LLC/DCX Transformers" — the volume-vs-loss trade-off on the frequency axis.
- "Core Loss under SiC/GaN: Datasheet vs Real Operating Point" — another source of estimation error.
- "AC Loss and Thermal Limits of Flat-Wire Windings in AI Servers" — the winding-side loss perspective.
- "AIDC 800V HVDC Bus Inductor Selection Guide" — a deeper look at the upstream stage of this chain.

Share Your Operating Conditions

- **We need:** Bus voltage and ratio (e.g. 48V→12V, N:1), switching frequency, duty / resonant operating point, target power and power density, temperature-rise and volume constraints.
- **We provide:** DCX core selection with iGSE loss calculation, planar/wire-wound route assessment, loss-thermal co-design and samples.
- **Contact:** Zhang Yong (Founder & Chief Engineer) | zyong@promagtech.cn | +86 13537658938 | www.promagtech.com

If the transformer loss and temperature rise at your 48V→12V stage are giving you trouble, send us your operating point — let us help you make this stage solid with engineering rather than guesswork.