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800 VDC Bus to 48 V: Magnetics Division of Labor in the AIDC Power Architecture

Filling the missing stage: how the 800 VDC bus itself gets built and stepped down to 48 V

Item	Detail
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Document	800 VDC Bus to 48 V — Magnetics Division of Labor in the AIDC Power Architecture
Scope	Magnetics at the 800 VDC bus stage and the isolated 800 V-to-48 V step-down for AI datacenter racks
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Summary & key takeaways

Bottom line

800 VDC is the core shift in next-generation AI datacenter power architecture — a DC bus replacing traditional 54 V rack-level and 480 VAC facility-level distribution to cut current and copper (NVIDIA has publicly stated roughly 45% lower copper use versus a 54 VDC rack architecture). The real gap for magnetics isn't the below-48V stages already covered (IBC/VRM) — it's the two stages nobody has written up yet: (1) where the bus itself comes from (grid/medium-voltage AC to 800 VDC), and (2) how the bus steps down to 48 V (a high-ratio, high-secondary-current isolation transformer). This article fills exactly those two stages.

Key takeaways:

- **800 VDC isn't just "a higher voltage":** at the same power, current drops sharply, so bus-level conductors and connectors can be thinner and lighter — a systemic reduction in current/copper, not merely a voltage parameter change.
- **The industry timeline is real:** NVIDIA's 800 VDC architecture is set to accompany its next-generation GPU platform, with per-rack power density targets already reaching the hundreds-of-kilowatts range — meaning bus-level magnetics will see current stress well beyond today's 48 V rack designs.
- **The bus has two evolving sourcing paths:** the conventional path steps grid power down through multiple AC-DC-AC-DC stages to 800 VDC; the more advanced path uses a solid-state transformer (SST) to convert 10–33 kV AC directly to 800 VDC in fewer stages.
- **The isolated 800 V-to-48 V step-down is this article's core new content:** a high turns ratio (~16–17:1) and very high secondary current make resonant converters (LLC/CLLC) with synchronous rectification the mainstream approach; the core design tension is leakage inductance control versus secondary-side conduction loss.
- **This chain shares core capability with EV/OBC 800V, but boundary conditions differ:** datacenter scenarios don't need automotive vibration/thermal-cycling qualification, but demand higher power density, current sharing across paralleled modules, and serviceability.

Note A ProMagTech engineering reference (not an official standard); the key supplement to the AIDC Full Power-Chain map, specifically covering the 800 VDC bus itself and the next isolation step-down that the map pointed to but never detailed — sister to the 1MHz Matrix Planar Transformer application note.

1. Why the "full power-chain map" alone isn't enough

ProMagTech's earlier AIDC Magnetic Components Full Power-Chain Applications mapped the path from 10 kV grid input through 800 V and 48 V down to CPU/GPU core voltages — but that's a navigation map, not a deep-dive. The bus-level stages (grid-to-800VDC, 800VDC-to-48V) are exactly the two segments the map marked but never expanded into selection methodology. This article's purpose: lay out the selection methodology for both stages and show how they connect to the deep-dives already published (1MHz Matrix Planar Transformer, IBC DCX).

2. Industry background for 800 VDC (why write this now)

NVIDIA has publicly disclosed an 800 VDC architecture aimed at replacing multi-stage 54 VDC rack-level and 480 VAC facility-level distribution with a DC bus, with officially stated copper reduction of roughly 45% versus a 54 VDC rack approach. This architecture is set to roll out alongside next-generation GPU platforms, with per-rack power density targets already reaching the hundreds-of-kilowatts range — meaning bus-level magnetics (rectification/conversion-stage inductors, isolated step-down transformers, bus-side CM filtering) will face current stress and power-density requirements well beyond today's 48 V rack designs.

Reminder 800 VDC is an architecture still evolving industry-wide; specific topologies and parameters from different vendors and standards bodies (e.g. the Open Compute Project) continue to develop. This article provides a general methodology framework, not the final architecture of any specific customer project.

3. Where the bus comes from: two evolving paths

Path	Conversion approach	Effect on magnetics
Conventional multi-stage path	grid (10 kV-class MV AC) → MV substation → 400/480 VAC → PFC rectification → 800 VDC	more conversion stages, each with its own magnetics (transformer/PFC inductor); higher total loss and footprint
Solid-state transformer (SST) direct path	10–33 kV AC converted directly to 800 VDC via power electronics, reducing intermediate transformer stages	requires a design approach for HV-side magnetics (high frequency, high-voltage isolation) entirely different from a conventional line-frequency transformer — a more advanced technology direction

Table 1 — Two evolving paths from grid power to the 800 VDC bus (specific approach depends on project/vendor)

For a magnetics manufacturer like ProMagTech, the PFC rectification-stage inductor in the conventional multi-stage path (interfacing 400/480 VAC front ends) and the high-frequency HV isolation stage in the SST path are two entirely different product requirements — the former extends naturally from existing industrial/PV PFC inductor capability, while the latter requires a new design with higher insulation class and higher frequency.

4. Bus to 48 V: the core design tension of the isolation step-down stage

This is the section closest to ProMagTech's core capability, and the one genuine gap in the previously published content matrix — selecting the transformer for an isolated 800 VDC-direct-to-48 V step-down. The core tension is clear:

Design variable	Tension	Direction
Turns ratio	800V→48V is roughly a 16.7:1 ratio; many primary turns, few secondary turns — leakage inductance and parasitic capacitance are harder to control	use matrix/multi-path parallel structures to split current rather than a single high-ratio winding

Secondary current	low voltage, high current — secondary-side loss dominates overall efficiency	synchronous rectification (SR) replacing diode rectification; flat-wire/busbar secondary windings
Resonant topology	LLC/CLLC resonant converters give the best efficiency across a wide load range, but demand tight transformer Lm/Lr precision	reuse the design methodology from the 800 V OBC CLLC Bidirectional Transformer article, adapted to the datacenter scenario
Power density	rack-level space is constrained; per-module power density requirements exceed automotive OBC	planar transformer structures (e.g. the published 1MHz Matrix Planar Transformer) are the mainstream direction

Table 2 — Core design tensions and directions for the 800V-48V isolation step-down transformer

Key The design methodology for this transformer stage strongly overlaps with the 800 V OBC CLLC Bidirectional Transformer article (resonant topology, Lm/Lr design, insulation design); the main difference is the datacenter scenario doesn't need bidirectional power flow but demands more from current sharing across paralleled modules and high-density packaging.

5. Bus-side EMI and common-mode considerations

The 800 VDC bus itself also needs common-mode filtering, particularly when the front end is high-frequency PFC/SST conversion rather than line-frequency rectification — see the material-by-band table in the EMI & Common-Mode Magnetics Pillar. Bus-level CM chokes typically fall in nanocrystalline's strong band (10 kHz–1 MHz) and must withstand DC bias current well beyond automotive scenarios.

6. Connecting to published content: the map is now complete

Chain segment	Coverage	Status
Grid to 800 VDC bus	§3 of this article (methodology framework)	new in this article
800 VDC bus to 48 V (isolation step-down)	§4 of this article + the 1MHz Matrix Planar Transformer app note (product-level deep-dive)	methodology filled by this article; deep-dive already published
48 V to 12 V (IBC stage)	IBC DCX Transformer Loss Analysis	published
48 V AI server PSU	48V AI Server PSU Flat Transformer Design Guide	published
12V/1V CPU/GPU VRM stage	covered by the AIDC Full Power-Chain map's navigation only, no dedicated deep-dive yet	candidate for future evaluation

Table 3 — AIDC full-chain content coverage status (after this article)

7. Validation & quality baseline (DVP)

Validation item	Method / instrument	Acceptance (example, per project)
Turns ratio / leakage / magnetizing inductance	LCR meter (short-circuit/open-circuit method)	target ± spec %
Secondary high-current loss / rise	ΔDCR method / IR camera	≤ spec limit
Current sharing across paralleled modules	multi-module parallel current distribution test	module-to-module deviation < spec %
Bus-side CM impedance	impedance analyzer (per EMI Pillar's material-by-band table)	Z ≥ spec across target band
Insulation design (bus-side HV)	per Insulation Design & PD Testing methodology	clearance/creepage + PDIV both meet spec
System-level efficiency (bus-to-48V stage)	efficiency curve (light load to full load sweep)	meets project efficiency target

Table 4 — Common validation baseline for 800VDC bus-to-48V magnetics (acceptance per project)

8. Frequently asked questions (FAQ)

Q Will 800 VDC architecture really be deployed at scale, or is it still conceptual?

A NVIDIA has publicly disclosed this architecture with an industry timeline tied to its next-generation GPU platform; specific topologies and standardization are still evolving — track ongoing developments from bodies like the Open Compute Project rather than treating this article as a finalized design.

Q Can the 800V-48V isolation transformer reuse the EV 800V OBC CLLC transformer design?

A The core design methodology (resonant topology, Lm/Lr, insulation design) overlaps heavily, but datacenter scenarios typically don't need bidirectional power flow and place more emphasis on current sharing and high-density packaging — expect targeted structural adaptation, not a direct part reuse.

Q Is the bus-side rectification/conversion inductor the same as existing PV/ESS PFC inductors?

A In the conventional multi-stage path, the design logic is very close to existing industrial/PV PFC inductors and can be treated as a capability extension; on the SST direct path, however, an entirely new high-frequency, high-voltage isolation design is required and cannot simply reuse existing designs.

Q How does an 800VDC bus-level CM choke differ from an automotive 800V platform CM choke?

A The band-division logic is the same (see the EMI Pillar's material-by-band table), but datacenter scenarios typically involve higher current and higher DC bias, requiring targeted recalculation of saturation behavior and winding structure rather than reusing automotive parameters directly.

Q Where does ProMagTech's delivery capability end on this chain?

A ProMagTech's core capability centers on the 800V-48V isolation step-down transformer (planar structure, matrix paralleling) and bus-level CM chokes; the grid-to-800VDC bus source stage — especially the SST path — is a more advanced technology direction requiring project-specific evaluation to confirm delivery scope.

9. Glossary

- **800 VDC architecture —** a datacenter power architecture using an 800 V DC bus in place of traditional 54 V rack-level and 480 VAC facility-level distribution.
- **Solid-state transformer (SST) —** a technology approach converting medium-voltage AC directly to a DC bus via power electronics, reducing conventional line-frequency transformer stages.
- **Matrix transformer —** a transformer design splitting a high-current secondary into multiple parallel paths to spread current and reduce per-path loss.
- **Synchronous rectification (SR) —** using low-conduction-drop power devices in place of diodes for rectification, reducing high-current secondary-side loss.
- **Current sharing —** how evenly current distributes across multiple power modules operating in parallel.

10. Further reading

- 1MHz / 3.3kW Matrix Planar Transformer Application Note (the product-level deep-dive for the 800V-48V isolation step-down)
- IBC DCX Transformer Loss Analysis (48V-12V stage)
- 48V AI Server PSU Flat Transformer Design Guide
- AIDC Magnetic Components Full Power-Chain Applications
- 800 V OBC CLLC Bidirectional Transformer Selection (isolation step-down design methodology reference)
- EMI & Common-Mode Magnetics — Selection Reference (Pillar)
- Insulation Design & Partial Discharge Testing — 800 V Platform Methodology

11. About ProMagTech

SHENZHEN PROMAGTECH CO.,LTD (founded 2013, Shenzhen) designs and manufactures planar transformers, flat-wire inductors and common-mode chokes for AI-datacenter power, 800 V EV OBC, PV inverters and energy-storage PCS.

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