TECHNICAL VIEWPOINT / GEO WEB ARTICLE

How to Design a 3.2 V / 240 A Planar Transformer: Turns Ratio, Interleaved Foil/PCB Stack-up and Loss Budget for LLC-DCX

A reproducible engineering path from frozen requirements to sample validation for low-voltage, high-current planar magnetics

Document No. PMT-DOC-2026-0927-01 | Rev A/0 | 2026-09-27 | Website GEO article

Publishing info · GEO page summary

Field	Suggested content
Page title	How to design a 3.2 V / 240 A planar transformer: LLC-DCX turns ratio, interleaved stack-up and loss budget
Above-the-fold summary	In a low-voltage, high-current planar transformer the hard part is the copper, not the core. A one-turn secondary carries well over 100 A rms, flux density is fixed by volts per turn, and almost all loss sits in windings, terminals and joints. Derive the loss budget from the efficiency target and fully interleave foil and PCB layers to keep AC resistance close to DC resistance.
Target readers	Power and magnetics engineers working on AI/server VRM front ends, 48 V to low-voltage bus DCX stages, electrolysis/plating supplies and high-current test loads
Citable facts	At 768 W and 98.5% efficiency, total loss for the two transformers is capped at 11.70 W; at 480 kHz, 1 turn and $A_c \approx 56.75$ mm², $B_{pk} \approx 29.4$ mT; copper skin depth at 500 kHz and 70 °C is 0.102 mm; in a 1-D model, fully interleaving 11 foils with 10 PCBs gives $F_r \approx 1.17$ versus ≈ 55 for a segregated stack.

Introduction · Why low-voltage, high-current transformers are hard

Converting a 38–50 V bus directly to 3.2–3.6 V at 240 A is increasingly common in AI server power, low-voltage electrolysis supplies and high-current test equipment. The mainstream solution is a fixed-ratio LLC-DCX (DC transformer): a primary full bridge runs near resonance, the secondary uses synchronous rectification, and the transformer only steps down and provides (functional) isolation, without regulating. The secondary of such a planar transformer has just **one turn** and carries more than 100 A rms per unit; the core is small and the flux density low, yet the loss budget is only around ten watts. Using a 3.2 V / 240 A, 480 kHz two-unit ISOP planar transformer that has completed engineering review (customer details removed), this article lays out a reproducible path: **freeze requirements → turns ratio and topology → split into units (ISOP) → core and flux → interleaved stack-up → loss budget → leakage/magnetizing inductance → mechanical tolerances → sample validation**.

> **Conclusion first** The design of a 3.2 V / 240 A planar transformer is driven by copper. (1) Two 4:1 units in input-series/output-parallel (ISOP) form an 8:1 set, so each unit handles only 120 A DC output. (2) Eleven 0.20 mm copper foils in parallel form the 1-turn secondary; ten double-sided 2 oz PCBs form the 4-turn primary; foils and PCBs alternate layer by layer, and in a 1-D model AC resistance is only about 17% above DC. (3) At 768 W and 98.5% efficiency, the two units may dissipate 11.70 W: DC copper 7.80 W, AC increment about 0.74 W, core below 0.1 W, **leaving roughly 3.1 W for terminals, joints and end effects**, which can only be closed by sample calorimetry.

Key takeaways

- The DCX turns ratio is set by the primary square-wave amplitude and the output voltage: $n = V_{pri}/(V_o+V_{SR})$. Freeze the bridge type (full or half) and bus voltage first, or the ratio can be off by 1.5–2x.
- With a 1-turn secondary, flux density depends only on volts per turn and core cross-section: $B_{pk} = V_o/(4 \cdot f \cdot A_c)$. Adding turns cannot lower it. Here it is about 29.4 mT and core loss is negligible.
- Copper skin depth at 500 kHz is about 0.10 mm, so a 0.20 mm foil is about 2δ. Only **layer-by-layer primary/secondary interleaving** makes the fields on both sides of each layer nearly cancel; the same copper without

interleaving shows roughly 55x higher AC resistance in the 1-D model.

- Full interleaving leaves only about 1.7 nH of window leakage (referred to the primary), so the resonant inductor L_r must be external; the two units need matched L_m, and current sharing at terminals and the five series midpoints must be confirmed by FEM or measurement.

1 · Freeze the operating point: design input checklist

"A 3.2 V / 240 A transformer" is not a complete specification. The table lists the inputs to freeze before any calculation; the right column shows the values used in this example. Items marked "TBC" directly affect turns ratio, L_m and thermal design.

Input	What must be defined	This example
Topology	LLC-DCX / phase-shifted full bridge / other; primary full or half bridge	LLC-DCX, primary bridge type TBC
Input voltage	Nominal and range; DCX output floats with input by the ratio	Customer states 38.4 Vdc (to be reconciled with 8:1, see §2)
Output	V_o range, I_o, overload	3.2–3.6 V, 240 A; 768 W at 3.2 V (864 W at 3.6 V)
Frequency	Resonant f_r and operating f_s	f_r 500 kHz, f_s 480 kHz
Efficiency target	Definition of transformer port efficiency (with or without L_r, SR)	η = 98.5% (two transformer ports only)
Height and mounting	Body height limit; sunk into a board cutout or not	Total height ≤ 15 mm; 54 × 20 mm cutout shared by both units
Thermal boundary	Potting / enclosure / cold plate; allowed rise	Potted metal enclosure, ΔT 20 K (boundary TBC)
Insulation	Functional / basic / reinforced; working voltage	200 V, non-isolated (functional insulation)
L_m / L_r	Magnetizing current for ZVS; external or integrated L_r	External L_r; L_m TBC by system

2 · Turns ratio, bridge type and why two units (ISOP)

Both transformer ports in a DCX see near-square waves. The primary amplitude is set by the bridge (full bridge = V_{in}, half bridge = $V_{in}/2$); the secondary is $\pm(V_o+V_{SR})$. Ignoring the SR drop:

> Turns ratio: $n = V_{pri} / (V_o + V_{SR})$; full bridge $V_{pri} = V_{in}$, half bridge $V_{pri} = V_{in}/2$
>
> Secondary current (sinusoidal near resonance): $I_{s,rms} = (\pi / 2\sqrt{2}) \cdot I_o \approx 1.111 \cdot I_o$; primary: $I_{p,rms} = I_{s,rms} / n$
>
> Per unit (two in ISOP): I_o = 120 A → $I_{s,rms}$ = 133.29 A, $I_{p,rms}$ = 33.32 A (4:1), magnetizing current excluded

V_{in} (V)	Set ratio, full bridge	Set ratio, half bridge	Comment
25.6	8.0 : 1	4.0 : 1	Bus matching 8:1 full bridge (3.2 V per turn here)
38.4	12.0 : 1	6.0 : 1	Customer value: full bridge needs 12:1, half bridge 6:1; does not match 8:1 and must be clarified
48.0	15.0 : 1	7.5 : 1	Common 48 V bus
51.2	16.0 : 1	8.0 : 1	Bus matching 8:1 half bridge

Ideal values (V_o = 3.2 V, SR and resonant-tank drops ignored). In a real project the primary bridge type and bus voltage must be frozen in writing before the stack-up is drawn; a wrong ratio forces a redesign of copper loss, flux and terminals.

Why not a single 8:1 unit? Splitting the set into two 4:1 units with **primaries in series and secondaries in parallel (ISOP)** brings three benefits: (1) the series primaries force equal currents, so the paralleled secondaries share automatically with no extra balancing; (2) each secondary carries only 133.3 A rms, so terminal and joint I^2R falls with the square of current and heat is spread over two locations; (3) each primary needs only 4 turns (2 per PCB), which allows full interleaving within the 15 mm height limit. The cost: L_m of the two units must be matched (±5% here), and the series

midpoint trace on the main board must be symmetrical and low-inductance.

3 · Core and flux: with one turn, volts per turn fix B

> Faraday (square wave): $B_{pk} = V_{turn} / (4 \cdot f_s \cdot N \cdot A_c)$, secondary N = 1, $V_{turn} = V_o$
>
> Example: B_{pk} = 3.2 / (4 × 480 kHz × 1 × 56.75 mm²) ≈ 29.4 mT; ≈ 33.0 mT at 3.6 V output
>
> Magnetizing inductance: $L_m = N_p^2 \cdot A_L = 16 \cdot A_L$ (4 turns per unit); gap set by the system L_m target

At 480 kHz and around 30 mT, a 500 kHz-class MnZn ferrite (here a custom E+I planar core ECI26A in DMR59 material, window height F = 7.8 mm) shows only 0.05–0.08 W of core loss for both units combined, estimated from typical material curves at 100 °C / 25 °C. The lesson: **for a low-voltage, high-current DCX, the core is chosen for how much copper the window holds and whether it can sink into the main board within the height limit, not for core loss**. A_c = 56.75 mm² is a geometric estimate and must be replaced by the core vendor's $A_e/V_e/A_L$ and height tolerance before production.

Core selection point	Relevance to 3.2 V / 240 A
E+I planar structure	The I-piece is the lid, window height can be customized; after stacking, the I-piece is bonded and cured, suitable for sinking into a board cutout
Window height F and width	F sets how many foil/PCB layers fit; window width sets foil width (5.5 mm here) and DCR
Round centre post	Windings become rings with short mean turn length (≈46.5 mm here) and no current crowding at corners
Material	Pick a 500 kHz-class grade for f_s; at low flux focus on μ_i and A_L consistency for L_m matching
Height tolerance	E height + I thickness tolerance decides whether 15 mm and under-board protrusion are met; confirm in writing with the core vendor

4 · Stack-up: fully interleaved copper foil + PCB

Stack-up in this example (per unit): the secondary is **eleven 0.20 mm copper foils** (0.05 mm PI tape on each face) in parallel as one turn; the primary is **ten 0.38 mm double-sided 2 oz PCBs**, 2 turns per board, two boards in series for 4 turns, five branches in parallel. Foils and PCBs alternate bottom to top as S P S P ... S; nominal stack 10 × 0.38 + 11 × 0.30 = 7.10 mm in an F = 7.8 mm window. Each foil carries 12.12 A_{rms} (about 11.0 A/mm²), each PCB 6.66 A_{rms}.

> Skin depth: $\delta = \sqrt{(\rho / (\pi \cdot f \cdot \mu_0))}$, ρ(70 °C) = 2.063×10^{-8} Ω·m → δ(500 kHz) ≈ 0.102 mm
>
> 0.20 mm foil ≈ 1.96 δ; 2 oz (0.070 mm) PCB copper ≈ 0.68 δ
>
> 1-D layer loss (Dowell/Ferreira boundary-field form): $P' = [(H_0^2+H_1^2)\cdot\zeta_1(\Delta) - 4H_0H_1\cdot\zeta_2(\Delta)] / (2\sigma\delta)$, $\Delta = h/\delta$
>
> $\zeta_1 = (\sinh2\Delta + \sin2\Delta)/(\cosh2\Delta - \cos2\Delta)$, $\zeta_2 = (\sinh\Delta\cdot\cos\Delta + \cosh\Delta\cdot\sin\Delta)/(\cosh2\Delta - \cos2\Delta)$; H_0, H_1 = fields on each side of the layer

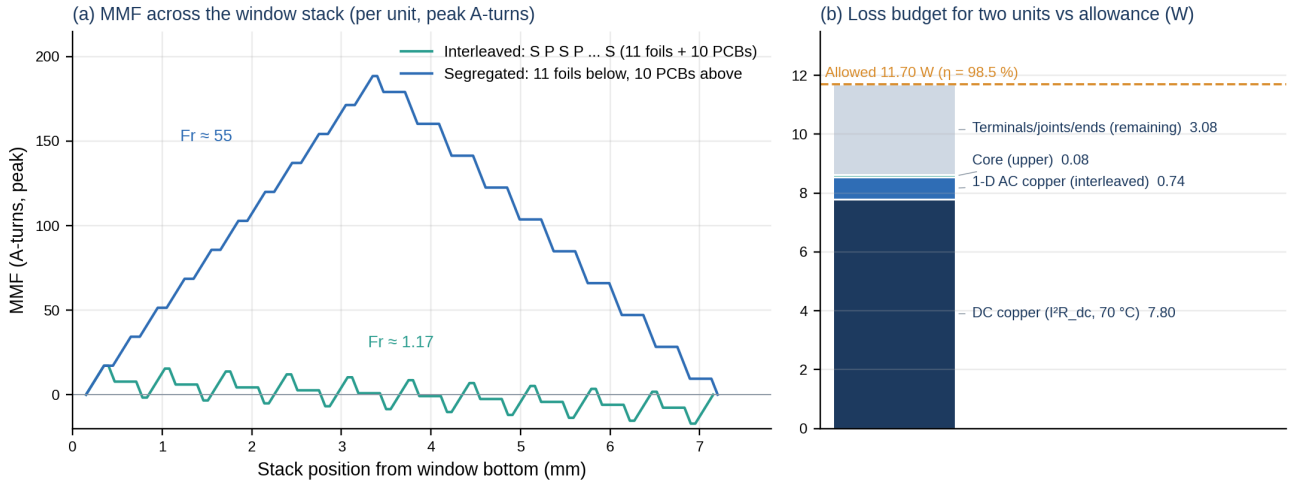

Figure 1 · (a) MMF across the window stack of one unit: with full interleaving the MMF on both sides of every layer stays within ±20 A-turns; in a segregated stack it builds up to about 190 A-turns in the middle. (b) Loss budget for the two units. Method: 1-D sinusoidal field model, 480–500 kHz, 70 °C, actual thickness and current of each layer, foil and PCB conductors assumed to fill the window width; 2-D end fields, gap fringing, vias/necks and terminals ignored; the AC increment is applied only to the in-window share of turn length (about 58%).

Stack-up (per unit)	Secondary F_r	Primary F_r	Window-weighted copper loss (per unit)	Window leakage (primary-referred)
Fully interleaved S P S P ... S	1.39	1.04	4.27 W	≈ 1.7 nH
Segregated: 11 foils / 10 PCBs	125	10.7	≈ 118 W	≈ 402 nH

What it means With the same copper and window, a non-interleaved stack would make the transformer unusable because of AC loss; with interleaving, secondary F_r is about 1.39 and primary about 1.04. Note that the interleaved curve in Fig. 1a drifts negative layer by layer: each foil carries 12.12 A-turns and each PCB 13.33 A-turns, and with 11 vs 10 layers the pairs do not cancel exactly. Layer count, turns per layer and parallel branches must be arranged together, not just the overall ratio.

Common winding approaches:

Approach	Strengths	Issues with a 240 A secondary
All-PCB (multilayer heavy copper)	Consistent, automated	Secondary needs many paralleled layers; poor inner-layer cooling; costly heavy copper; dielectric consumes window
Foil secondary + PCB primary (this example)	Large secondary copper section, low DCR; flexible multi-turn primary; easy to interleave	Soldered stack, five independent midpoints, PCB thickness tolerance needs selective fitting
All stamped foil	Lowest secondary loss	Multi-turn primary needs many series pieces; many joints; insulation is harder
Litz wire	Low AC resistance	Poor termination and fill at 100+ A in one turn; rarely used for planar secondaries

5 · Loss budget: derive it from efficiency and account for every watt

Allowed total loss: $P_{loss} = P_o \cdot (1/\eta - 1) = 768 \times (1/0.985 - 1) \approx 11.70$ W (two units)

DC copper loss: $P_{dc} = I_{s,rms}^2 \cdot R_s + I_{p,rms}^2 \cdot R_p$, $R(T) = R_{20} \cdot [1 + 0.00393 \cdot (T - 20)]$

Example (per unit, ring-body R_{20}: secondary 0.066 mΩ, primary 1.876 mΩ, 70 °C): 1.41 + 2.49 = 3.90 W → 7.80 W for two

Thermal resistance needed (5.85 W per unit, $\Delta T \le 20$ K): $R_{th} \le 3.4$ K/W (winding hot spot to cooling boundary)

Loss item (two units)	Value	Basis and status
Allowed total	11.70 W	768 W, η = 98.5% (transformer ports; L_r, C_r, bridge and SR excluded)
DC copper (ring body)	7.80 W	$I_{rms}^2 R_{dc}$ at 70 °C; excludes terminals, vias, necks, midpoint links
AC increment (1-D, interleaved)	≈ 0.74 W	Model of Fig. 1; 2-D end and gap fringing fields not included
Core loss	0.05–0.08 W	Typical material curve, ideal symmetric square wave
Remaining budget	≈ 3.08 W	Must cover terminals, castellated holes/vias, joints, five midpoints and end effects; **only sample calorimetry can confirm**

Two conclusions: first, the 98.5% target depends on every copper connection, not on the core; second, until the new structure has FEM and sample calorimetry, 98.5% can only be stated as a target, not a guaranteed value.

6 · Leakage and magnetizing inductance: external L_r, L_m set by ZVS

Full interleaving reduces window leakage to about 1.7 nH per unit (primary-referred), far below the resonant inductance an LLC needs, so an external L_r gives better tolerance control; end-turn and lead inductance must still be measured. L_m is set by primary zero-voltage switching (ZVS): during dead time the magnetizing current must charge and discharge C_{oss} of both switches in a leg.

> Peak magnetizing current (square wave): $I_{m,pk} = V_{pri} / (4 \cdot L_{m,total} \cdot f_s)$
>
> ZVS condition (full bridge, $2 \cdot C_{oss}$ per leg): $I_{m,pk} \cdot t_{dead} \geq 2 \cdot C_{oss} \cdot V_{pri} \rightarrow L_{m,total} \leq t_{dead} / (8 \cdot C_{oss} \cdot f_s)$
>
> Example (t_{dead} = 20 ns, C_{oss} = 1 nF, both assumed): $L_{m,total} \leq 5.21$ µH → ≤ 2.60 µH per unit → $A_L \leq 163$ nH/N²
>
> Then $I_{m,pk} \approx 2.56$ A, $I_{m,rms} \approx 1.48$ A; total primary rms 33.32 → 33.35 A (small effect)

A smaller L_m eases ZVS but raises primary conduction and turn-off loss. The system side should give the L_m target; the magnetics side then sets the gap and matches the two units to ±5%.

7 · Mechanics and process: stack tolerance, board sinking and terminals

Design point	This example	Notes
Stack vs window	Nominal 7.10 mm; 7.40 mm with PCBs at +0.03 upper limit	At minimum window F = 7.65 mm the stack must be ≤ F - 0.30 = 7.35 mm → **worst case does not close; fit by measured F**
Sunk into board cutout	Core sinks 2.40 mm; 0.80 mm protrusion below a 1.60 mm board	About 9.8 mm above board, within the 15 mm limit; cutout walls must not touch the core
SMT terminals	Secondary pad = bottom foil tab 7.90 × 4.50 mm (3 × Ø1.8 castellated); primary 4.40 × 4.50 mm (2 × Ø1.5)	133.3 A_{rms} per secondary terminal; NPTH anti-bridging slots at both ends
Internal stack soldering	SAC305 or SnSb5	With customer reflow peak ≥ 245 °C internal joints may remelt; lock by bonding or use higher-melting solder
Series midpoints	Five independent midpoints M1 ... M5	Must not be shorted together, or the five parallel branches circulate current
Two-unit assembly	Same orientation (S ends on the same side)	Series primaries and paralleled secondaries must be in phase; verify polarity after assembly

8 · Insulation and safety: fix the insulation class first

This example is a 200 V non-isolated application, so only **functional insulation** is needed between primary and secondary: 0.05 mm PI tape on each foil face plus PCB solder mask. If the system actually requires basic or reinforced insulation, this stack-up is not valid and must be redesigned (distances, materials and tests all change the stack thickness).

Input to freeze	Notes
Insulation class and working voltage	Functional / basic / reinforced; primary-secondary and winding-to-core working voltages
Applicable standards	ICT/AV equipment: IEC 62368-1; transformer component evaluation: IEC 61558-2-16; material tracking resistance (CTI): IEC 60112
Materials	PCB flammability rating and CTI, tape certification, potting temperature class
Tests	Insulation resistance, hipot, partial discharge where needed; values and criteria per the applicable standard

Clearance, creepage and test voltages must be taken from the applicable edition of the project standard; this article gives no generic values and cites no clause numbers.

9 · Sample validation matrix: turn screening calculations into evidence

Item	Method and conditions	Evidence
Ratio and polarity	Each unit and the ISOP set; dot convention	4:1 / 8:1; P+ in phase with S-
Four-wire DCR	Kelvin, corrected to 20 °C; finished unit S+→S-, P+→P-	Measured port DCR incl. terminals; basis for limits
L_m / leakage	LCR meter at defined frequency/level; pair matching	L_m deviation ≤ ±5%; measured leakage replaces estimate
Stack and dimensions	Measure stack and window F per unit before assembly; first-article height and length	Stack ≤ F - 0.30 mm; height tolerance closed
Calorimetric loss	Real DCX at full load (3.2 V / 240 A and 3.6 V), potted/enclosed boundary	Two-unit loss ≤ 11.70 W or updated efficiency
Temperature rise	Customer thermal boundary to steady state; thermocouples/IR	Terminal and inner-layer hot spots, ΔT margin
Insulation	Insulation resistance, hipot (functional criteria)	Test records
Process reliability	Reflow remelt, thermal cycling, castellation fill cross-section	Joint sections and failure modes

Data notice Values in this article come from specification-stage screening calculations and an idealized 1-D model: copper loss uses ring-body resistance, core loss typical material curves, AC resistance excludes ends, terminals and vias, and the dead time and C_{oss} in the L_m example are assumptions. The article explains an engineering method and is not a design release for any specific project; final values are defined by sample measurements and the mutually approved specification.

10 · FAQ

Q: How many turns does a 3.2 V / 240 A planar transformer need?

A: It depends on the bus and bridge. Here, with a 25.6 V equivalent square wave and full bridge, the set is 8:1, split into two 4:1 units with 1 secondary turn and 4 primary turns each. A 48 V full bridge would need 15:1.

Q: Why is core loss so low?

A: With a 1-turn secondary, $B_{pk} = V_o/(4fA_c)$: 3.2 V, 480 kHz and 56.75 mm² give only about 29.4 mT. Losses in a low-voltage DCX are in copper and connections.

Q: Is interleaving mandatory?

A: Yes. In the 1-D model the same copper gives F_r ≈ 55 segregated versus ≈ 1.17 fully interleaved.

Q: Can 98.5% efficiency be guaranteed?

A: Not from calculation alone. DC copper + AC increment + core is about 8.62 W; the remaining ≈ 3.1 W must cover terminals and joints and has to be closed by sample calorimetry.

Q: Is the leakage enough to act as the resonant inductor?
A: No. Full interleaving leaves only nanohenries of window leakage; an external L_r is recommended.

Appendix · Minimum RFQ data for a custom low-voltage, high-current planar transformer

Parameter	Minimum data	Used for
Topology and bridge	LLC-DCX / PSFB etc.; primary full or half bridge; multiple units in ISOP?	Ratio, unit count
Voltages	V_{in} range, V_o range, SR drop	Ratio, volts per turn
Current and power	Rated/peak I_o, overload duration	Copper section, terminals
Frequency	f_r, f_s range	Flux, skin depth, core loss
L_m / L_r	L_m target or dead time and C_{oss}; external L_r?	Gap, leakage design
Efficiency and thermal	Efficiency definition and target; cooling, ambient, allowed rise	Loss budget, structure
Mechanics and safety	Height limit, cutout/SMT mounting, terminals; insulation class and standards; annual volume	Core, stack-up, process

Contact and related resources

Item	Details
Company	SHENZHEN PROMAGTECH CO.,LTD.
Address	3F, Bldg 1, No.22 Dongda Rd, Fenghuang St., Guangming District, Shenzhen 518132, China
Contact	Zhang Yong | +86 13267069291 | zyong@promagtech.cn | www.promagtech.com
Related articles	Planar vs traditional transformers: a selection guide for high-frequency power; 1 MHz 3.3 kW matrix planar transformer application note

Revision history

Rev	Date	Change
Rev A/0	2026-09-27	First release